Pixel FE Electronics Status

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Summarize current understanding of chips from recent DMILL submission:

- Major effort devoted to FE-D front-end chip. Several design problems found, but now fairly well characterized and agree with simulation results. Several serious problems remain, which we attribute to fabrication.
- Other devices in run work, with exception of DORIC-p, which has real problems.
- Near future plans include processing 4 backup wafers to investigate yield problems, followed by a new engineering run with all known errors fixed.

Presently also working on Honeywell SOI version of FE chip

- Layouts of some blocks done. Indications are good for 300μ B-layer pixel size.

Summary of Recent DMILL Reticle

Reticle included many die (10 in total):

- Two pixel FE chips (FE-D). Present status is that several errors have been found and reproduced in simulation. Several other significant problems are believed to originate in TEMIC fabrication problems
- Prototype MCC chip. A prototype of several key elements of final MCC, about 20mm^2 core size. Includes FIFO block for final chip, plus large synthesized command decoder block. Presently have tested 14 die, of which 11 work. Appear to be no problems with this design, but more complete testing underway.
- Prototype CMOS opto-link chips (one DORIC-p and three VDC-p). VDC-p seems to work well up to about 150MHz. DORIC-p has several problems which are not presently understood.
- Additional test chips: LVDS buffer for rad-hard test board, PM bar with W/L arrays and special pixel transistors, Analog Test chip with all critical FE-D analog elements. All work well, and transistor parameter measurements suggest the run is slightly faster than typical. Many detailed characterizations of Analog Test Chip.
- Plan to irradiate at least several of the test chips to relevant doses in April in PS.

Testing still continuing...

What works in FE-D:

Answer: Almost everything works from the design point of view:

- Studies of analog blocks, including current reference, current and voltage DACs, internal calibration circuit, etc. indicate all behave well, with exception of one layout error in VTH Amplifier block.
- Analog performance is very close to what we expect in terms of shaping time, noise and threshold dispersion, timewalk performance, charge measurements, etc. Performance not yet confirmed with bump-bonded assemblies - delivery of single chips from both bumping vendors expected within 2 weeks. Many system level measurements now made, as well as individual blocks. Some systematic effects seen and under study (e.g. TOT charge calibration has large left-right variation).
- Digital readout works well, including data transfer from column pairs at 20 MHz, with signal recovery at bottom of column by sense amplifiers. Data transfered from chip is correct under almost all circumstances. Major problem is high VDD required for correct operation. This is now understood.
- Power consumption of many blocks studied for DC and as a function of XCK frequency. For some chips, the agreement with expectations is very good.

Summary of FE-D Design Errors

Analog:

- VTH amplifier layout error (mistake not caught due to design kit error). Presently fixed by FIB surgery.

Integration:

- Basic problem: Missing or mis-sized buffers in several critical locations. Clearly, we are reviewing buffer sizing in detail for the entire chip.
- Several buffers for control logic were undersized, so some commands must be “slowed down” in software.
- Two critical clocks (XCK, CLK1/CLK2) not distributed with adequate buffering, but simulations and measurements indicate these errors are dangerous but not fatal in pre-rad chip operation.
- Missing buffer in serial output stream. This causes data corruption unless VDD supply increased to maximum value permitted by process (about 5V). Have verified using FIB surgery that bringing this signal out directly using an active probe allows us to operate the full chip correctly with VDD = 3.0V.
- Missing connection to one address pad. Mistake not caught due to design kit error.

Digital Readout:

- Missing column masking on Buffer Overflow OR tree.

Serious problems not attributed to design errors:

- Very poor yield on Pixel Register (2880 bit register in pixel matrix used for individual pixel control).
- Note this register is “quasi-static” in order to reduce transistor count. Extensive analysis examined behavior of defective pixels as a function of VDD, clock frequency and duty cycle, and made detailed comparisons with simulations. Yield is about 0.3 for 3mm^2 of circuitry. Very good consistency with a model in which a particular PMOS has a defect rate of 1:5000, with the defect being a drain-source resistance of several megohms.
- Defective pixels which cause peculiar digital “oscillations” in the column-pair readout circuitry. Detailed studies of behavior, and comparisons with simulations, suggest a problem with a defective NMOS, also with a drain-source resistance of several megohms. Here, the defect rate is much higher, about 1:200.
- Significant number of chips with anomalous digital power consumption.
- Result is that our yield for chips which pass even simple digital checks is essentially zero (very similar chip in rad-soft process had 92% yield over 20 wafers, with much more sophisticated testing).

Next Steps for FE-D

- Work on list of action items from recent TEMIC visit, mainly trying to measure MOS defects using FIB modifications to prove they are not design faults.
- Continue characterizations to see if there is “fine-tuning” of analog section to do. Also continue trying to understand lack of stability associated with Resets.
- Characterize bump-bonded assemblies as soon as they return (may require additional surgery on some to make SDO mod to allow 3.0V VDD operation).
- Work on modifications for backup wafer run. The M1 and M2 masks are not needed immediately and will implement debugging aids and minor fixes. This run should take 4-6 weeks to return, and we will most likely wait for these wafers before sending in FE-D2.
- Complete presently known modifications to FE-D design database to make FE-D2. List of changes is quite modest (but critical !).
- Continue intensive simulation and verification work on FE-D2 database.
- Do PS irradiations on PM bars and Analog Test chips to validate performance of individual devices and analog portions of FE-D under irradiation.
- Actual submission date for FE-D2 will depend on factors above, but should be as early as possible (during March) to allow us to complete serious evaluation this Summer (PS and other irradiations, single-chip and module assemblies, testbeams, etc.). Several activities may not be completed by submission date.

Summary of Status of FE-H (Honeywell SOI version)

- Infrastructure work almost done (Standard Cell library, Cadence files, etc.), and last concerns about completeness of "new" Layout Rules scheme now seem to be resolved.
- Transfer agreements with collaborators "essentially" in place. Honeywell in process of shipping relevant documentation so Bonn and Marseille can begin design contributions immediately.
- First significant work on layout for digital readout (2x16 pixel block) indicates we can improve on several aspects of FE-D, while achieving the 300μ pixel size we want for the B-layer. This is due to smaller device size and closer packing, plus third metal layer.
- Effort on FE-H is presently significantly reduced due to activity in understanding FE-D and submitting FE-D2. This is certainly generating delay. Hope to begin engineering run by mid-Summer.